VDPC3005 VLSI FABRICATION TECHNOLOGY (3-0-0)

Course Objectives:

This course aims to provide students with a comprehensive understanding of the fundamental steps involved in semiconductor device and integrated circuit fabrication. It covers silicon wafer preparation, oxidation, diffusion, ion implantation, photolithography, etching, thin-film deposition, and isolation techniques. Students will also learn the basics of CMOS process integration, packaging, and reliability, enabling them to appreciate fabrication constraints, design limitations, and technological trade-offs in VLSI manufacturing.

Module–I: Silicon Wafer Processing & Epitaxy (06 Hours)

Introduction to IC fabrication process flow (BJT/MOSFET/CMOS), Cleanroom concepts, contamination control, wafer cleaning (RCA). Silicon crystal structure, defects, dislocations; Czochralski and Float-Zone crystal growth, ingot slicing, wafer lapping and polishing, wafer gettering. Basics of Epitaxy: Purpose of epitaxial layers, Vapor Phase Epitaxy (VPE), and introductory concepts of MBE and MOCVD (overview).

Module–II: Oxidation, Diffusion & Ion Implantation (06 Hours)

Thermal oxidation of silicon: dry vs wet oxidation, oxide quality and applications (gate oxide, masking oxide). Diffusion of dopants: constant-source and limited-source diffusion, junction depth formation (conceptual), role of diffusion in IC fabrication. Ion implantation fundamentals: dose, energy, ion range (conceptual), implantation damage, need for annealing, Rapid Thermal Annealing (RTA) for dopant activation.

Module–III: Photolithography & Etching Techniques (06 Hours)

Photolithography: photoresists (positive/negative), soft bake, exposure, development, mask alignment, resolution limits (basic). Overview of advanced lithography: e-beam lithography, EUV (conceptual). Etching techniques: wet etching (isotropic/anisotropic), plasma etching, Reactive Ion Etching (RIE), etch selectivity and material-dependent etching behavior.

Module–IV: Thin-Film Deposition & Device Isolation (06 Hours)

Thin-film deposition techniques: CVD processes (APCVD, LPCVD, PECVD), PVD methods (evaporation, sputtering); dielectric deposition (SiO_2, Si_3N_4), basic metal deposition (Al, Cu). Device isolation techniques: oxide isolation, LOCOS (limitations), introduction to Shallow Trench Isolation (STI). Planarization: Chemical Mechanical Polishing (CMP) – concept and applications.

Module–V: CMOS Process Integration, Packaging & Reliability (06 Hours)

CMOS process flow: NMOS, PMOS, and CMOS fabrication sequence; well formation, threshold voltage adjustment (concept), polysilicon gate formation. Formation of LDD structures, sidewall spacers, silicide formation, interconnects (metal layers, vias). VLSI packaging fundamentals: DIP, QFP, BGA, flip-chip packaging; thermal considerations, yield, contamination control. Reliability issues: electromigration, introduction to oxide breakdown.

Course Outcomes:

After completion of the course, students will be able to:

CO1: Describe the major steps involved in semiconductor device and IC fabrication.
CO2: Explain the principles of oxidation, diffusion, ion implantation, lithography, etching, and thin-film deposition.
CO3: Identify material, thermal, and process limitations that impact device performance.
CO4: Understand CMOS process integration and device isolation techniques.
CO5: Recognize packaging requirements and basic reliability concerns in VLSI manufacturing.

Text Books:

1. James D. Plummer, Michael Deal, Peter Griffin, Silicon VLSI Technology, Prentice Hall.
2. Sorab K. Gandhi, VLSI Fabrication Principles, Wiley.
3. S. M. Sze, VLSI Technology, McGraw-Hill.

References:

1. Stephen A. Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press.
2. Peter Van Zant, Microchip Fabrication: A Practical Guide to Semiconductor Processing.
3. Relevant NPTEL courses from IIT Bombay, IIT Madras, IIT Kharagpur.