VDPC3004 VLSI TESTING (3-0-0)

Course Objectives:

1. To introduce the fundamentals of VLSI testing, fault models, test generation, and fault coverage analysis.
2. To provide knowledge on design-for-testability (DFT) techniques including scan architectures, fault simulation, and structured DFT methodologies.
3. To familiarize students with Built-in Self-Test (BIST) concepts, ATPG algorithms, LFSRs, MISRs, and various test generation and compression techniques.
4. To develop understanding of boundary scan standards, delay testing, mixed-signal testing, FPGA testing, and testing of emerging devices such as MEMS and RF circuits.
5. To impart foundational knowledge of verification techniques including simulation-based, analytical, and formal verification, along with equivalence and model checking principles.

Module 1: Introduction to VLSI testing: Importance of testing, Challenges in VLSI testing, Levels of abstractions in VLSI testing, Functional vs. Structural approach to testing, Complexity of the testing problem, Controllability and Observability, Generating test for a single stuck at fault in combinational logic, D-algorithm, FAN and PODEM algorithms, Test optimization and fault coverage. (6 Hours)

Module 2: Design for testability (DFT): Testability analysis, Scan cell design, Scan architectures, Scan design rules, Scan design flow, Special purpose scan designs Logic and fault simulation, Fault detection, Adhoc and structured approaches to DFT, Various kinds of scan design, Fault models for PLAs, Bridging and delay faults and their tests. (6 Hours)

Module 3: Built-in self-test (BIST): Random test generation, Boolean difference, ATPG algorithms for combinational circuits, Sequential ATPG, Untestable faults, IDDQ testing The LFSRs and their use in random test generation and response compression (including MISRs) (6 Hours)

Module 4: Boundary scan: IEEE standards for digital boundary scan, Embedded core test standards Analog and mixed signal testing, Delay testing, Physical failures, FPGA testing, MEMS testing, RF testing, High speed I/O testing. (6 Hours)

Module 5: Verification techniques: Importance of verification, Verification plan, Verification flow, Levels of verification, Verification methods and languages, Introduction to Hardware Verification methodologies, Verifications based on simulation, analytical and formal approaches. (6 Hours)

Course Outcome:

CO1: Able to carry out research and development in the area of testing and verification of VLSI circuits.
CO2: Apply techniques to improve testability of VLSI circuits.
CO3: Utilize logic simulation methods, ATPG, BIST and boundary scan techniques in testing of VLSI circuits.
CO4: Apply functional, timing and formal verification methods at various design abstractions of VLSI circuits.
CO5: Solve practical and state of the art testing and verification problems to serve VLSI industries

Text Book:

1. Parag K. Lala, An Introduction to Logic Circuit Testing, Morgan & Claypool Publishers
2. Thomas Kropf, Introduction to Formal Hardware Verification, Springer.

Reference Books:

1. Michael L. Bushnell and Vishwani D. Agrawal, Essentials of Electronic Testing, Springer India
2. M. Abramovici, M. Breuer, and A. Friedman, Digital System Testing and Testable Design, Jaico Publishing House