| 4th Semester | RIT4C003 | Computer Organization and Architecture | L-T-P 3-0-0 | 3 CREDITS |
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**Objectives of the course:**

To expose the students to the following:

1. How Computer Systems work & the basic principles
2. Instruction Level Architecture and Instruction Execution
3. The current state of art in memory system design
4. How I/O devices are accessed and its principles.
5. To provide the knowledge on Instruction Level Parallelism
6. To impart the knowledge on micro programming
7. Concepts of advanced pipelining techniques.

**Module-I:** **(8 Hrs.)**

**Functional blocks of a computer**: CPU, memory, input-output subsystems, control unit. Instruction set architecture of a CPU–registers, instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set. Case study – instruction sets of some common CPUs.

**Module-II:** **(08 Hrs.)**

**Data representation**: signed number representation, fixed and floating point representations, character representation. Computer arithmetic – integer addition and subtraction, ripple carry adder, carry look-ahead adder, etc. multiplication – shift-andadd, Booth multiplier, carry save multiplier, etc. Division restoring and non-restoring techniques, floating point arithmetic.

**Module-III:** **(12 Hrs.)**

**Introduction** to x86 architecture.

**CPU control unit design**: hardwired and micro-programmed design approaches, Case study – design of a simple hypothetical CPU.

**Memory system design**: semiconductor memory technologies, memory organization.

**Peripheral devices and their characteristics**: Input-output subsystems, I/O device interface, I/O transfers–program controlled, interrupt driven and DMA, privileged and non-privileged instructions, software interrupts and exceptions. Programs and processes–role of interrupts in process state transitions, I/O device interfaces – SCII, USB

**Module-IV:** **(07 Hrs.)**

**Pipelining**: Basic concepts of pipelining, throughput and speedup, pipeline hazards.

**Parallel Processors**: Introduction to parallel processors, Concurrent access to memory and cache coherency CPU Basics: Multiple CPUs, Cores, and Hyper-Threading, Introduction to Multiple-Processor Scheduling in Operating System.

**Module-V:** **(08 Hrs.)**

Memory organization: Memory interleaving, concept of hierarchical memory organization, cache memory, cache size vs. block size, mapping functions, replacement algorithms, write policies.

**Books:**

- "Computer Organization and Design: The Hardware/Software Interface", 5th Edition by David A. Patterson and John L. Hennessy, Elsevier.
- "Computer Organization and Embedded Systems", 6th Edition by CarlHamacher, McGraw Hill Higher Education.

- "Computer Architecture and Organization", 3rd Edition by John P. Hayes, WCB/McGraw-Hill
- "Computer Organization and Architecture: Designing for Performance", 10th Edition by William Stallings, Pearson Education.
- "Computer System Design and Architecture", 2nd Edition by Vincent P. Heuring and Harry F. Jordan, Pearson Education.

**Course outcomes**

1. Draw the functional block diagram of a single bus **architecture of a computer and describe the function of the** instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set.
2. **Write** assembly language program for specified microprocessor for computing 16 bit multiplication, division and I/O device interface (ADC, Control circuit, serial port communication).
3. Write a flowchart for Concurrent access to memory and cache coherency in **Parallel Processors** and describe the process.
4. Given a CPU organization and instruction, design a memory module and analyze its operation by interfacing with the CPU.
5. Given a CPU organization, assess its performance, and apply design techniques to enhance performance using pipelining, parallelism and RISC methodology