PET8J003 ELECTRONIC DESIGN AUTOMATION

MODULE-I

MOSFET small signal model, MOSFET parasitic capacitance value and modification in model. Scaling of MOS structure; SPICE level -1, level-2 and level 3 model; BSIM and CSIM models; Comparison between models. Layout generation, Design checking rules, Lamda, beta rule, routing: auto routing,

MODULE-II

Advance programming using VHDL. Component level programming. Library files, type\ declaration and usage, parameter types and overloading, types and type related issues, predefined and user-defined attributes, package declaration and usage.

MODULE-III

Introduction to CADENCE, Use of CADENCE, Basic modeling using CADENCE, Layout generation using CADENCE. Introduction to low power IC design using CAD tools,

MODULE-IV

Delta delay modeling, insertion and transport delay. Use of signal drivers. Multiple processes

ADDITIONAL MODULE (Terminal Examination-Internal)

Device floor planning basics, Case study of a low power OPAMP design and layout generation.

Text book

1. Electronics Design Automation: Synthesis, verification & Test (System on Silicon)- Laung-Terng Wang, Morgan Kaufmann,2009
2. Essential Electronics design Automation (EDA)- Mark D.Birnbaum, Prentice Hall,2004