ASIC and SoC Design (3 – 0 – 0)

MODULE – I **(11 hours)**

Introduction: Voice over IP SOC, Intellectual Property, SOC Design Challenges, Design Methodology.

Overview of ASICs: Introduction, Methodology and Design Flow, FPGA to ASIC Conversion, Verification.

MODULE – II **(11 hours)**

SOC Design and Verification: Introduction, Design for Integration, SOC Verification, Set-Top-Box SOC, Set-Top-Box SOC Example. Summary. References.

Physical Design: Introduction, Overview of Physical Design Flow, Some Tips and Guidelines for Physical Design, Modern Physical Design Techniques.

MODULE – III **(12 hours)**

Low-Power Design: Introduction, Power Dissipation, Low-Power Design Techniques and Methodologies, Low-Power Design Tools, Tips and Guidelines for Low-Power Design.

Low-Power Design Tools: PowerTheater, PowerTheater Analyst, PowerTheater Designer.

Open Core Protocol (OCP): Highlights, Capabilities, Advantages, Key Features.

Phase-Locked Loops (PLLs): PLL Basics, PLL Ideal Behavior, PLL Errors.

Text Books:

3. Farzad Nekoogar and Faranak Nekoogar, ***From ASICs to SOCs: A Practical Approach***, Pearson Education, 2003, ISBN-10: 0-13-033857-5, ISBN-13: 978-0-13-033857-0

Recommended Reading:

5. Michael Smith, ***Application Specific Integrated Circuit***, Addison-Wesley, 1997, ISBN: 0201500221
6. Jari Nurmi, ***Processor Design: System-On-Chip Computing for ASICs and FPGAs***, Springer, 1st edition, 2007, ISBN: 1402055293
7. Douglas J. Smith, ***HDL Chip Design*** – a practical guide for designing, synthesizing and simulating ASICs and FPGAs using VHDL or Verilog, Doone Publications, 2000, ISBN: 0965193438