EOPC3005 VLSI DESIGN (3-0-0)

Course Objectives

This course introduces students to the fundamentals of CMOS-based VLSI circuit design. It covers MOS transistor operation, CMOS inverter characteristics, digital logic gate design, sequential circuit implementation, and HDL-based modeling using Verilog. Students will gain foundational knowledge of RTL design and synthesis methodology, enabling them to understand modern VLSI design flows used in industry.

Module–I: Introduction to VLSI Design & CMOS Technology (06 Hours)

Introduction to VLSI design, abstraction levels, VLSI system hierarchy, regularity, modularity, and locality. Overview of VLSI design styles, quality metrics such as area, delay, power, and reliability. VLSI design flow from behavioral description to physical implementation. Basic CMOS technology concepts, n-well/p-well processes, layout fundamentals including stick diagrams and design rules.

Module–II: MOS Transistor Fundamentals & CMOS Inverter (06 Hours)

MOSFET structure and operation, threshold voltage concepts, MOS I–V characteristics (conceptual), body effect and channel length modulation (introductory). CMOS inverter principles, voltage transfer characteristics (VTC), noise margins, power dissipation components. Dynamic behavior of the CMOS inverter including rise/fall times, propagation delays, and capacitive loading.

Module–III: CMOS Logic Design (06 Hours)

Design of static CMOS logic gates such as NAND, NOR, XOR, and complex logic structures. Transmission gate logic and pass-transistor logic for efficient combinational circuit realization. Implementation of multiplexers, adders, and basic arithmetic circuits. Sequential logic circuit fundamentals including latches, flip-flops, registers, and timing constraints. Concepts of setup time, hold time, clock skew, jitter, and their impact on synchronous system performance.

Module–IV: Verilog HDL Programming (06 Hours)

Introduction to Verilog HDL: modules, ports, data types, nets, and registers. Behavioral, dataflow, and structural modeling styles. Combinational circuit design using continuous assignment and procedural blocks. Sequential logic implementation using always blocks, blocking/non-blocking assignments, and event control. Writing Verilog testbenches for simulation, waveform analysis, and verification of functionality.

Module–V: RTL Design & Synthesis Flow (06 Hours)

RTL-level digital system design, synthesizable Verilog constructs, FSM design using Verilog (Moore and Mealy models). Design examples such as counters, shift registers, ALU components, and control FSMs. Introduction to logic synthesis, technology mapping, resource utilization, and timing reports.

Course Outcomes

Upon completion of the course, students will be able to:

CO1 Understand MOS transistor behavior, CMOS inverter characteristics, and design metrics.
CO2 Analyze and design basic CMOS combinational and sequential logic circuits.
CO3 Develop synthesizable Verilog HDL for digital systems.
CO4 Design and simulate RTL blocks and finite-state machines.
CO5 Understand synthesis, technology mapping, and FPGA implementation flow.

Text Books

1. Jan M. Rabaey, Digital Integrated Circuits: A Design Perspective, Pearson.
2. Neil H. E. Weste & David Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Pearson.
3. Kang &Leblebici, CMOS Digital Integrated Circuits, McGraw-Hill.

References

1. John Uyemura, Introduction to VLSI Circuits and Systems.
2. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis.
3. NPTEL Courses: CMOS Digital VLSI Design, Digital IC Design.