VLSI

Pre-requisites (if any): Basic Electronics, Digital Electronics, Microprocessors and Microcontrollers

Course Objectives:

1. Acquire knowledge about VLSI design, VLSI packaging and fabrication.
2. Study different partitioning algorithms.
3. Obtain knowledge on various floor planning techniques for efficient floor plan.
4. Understand the requirement of placement for good packaging.
5. Know about different routing algorithms for efficient communication.

Module I (6 Hrs)

VLSI Physical Design: VLSI Design Cycle, Physical Design Cycle, Design styles: Full custom, Standard Cell, Gate Arrays, FPGA, System Packaging Styles: Die Package Style, PCB, Multichip Modules, Wafer Scale Integration, Design Rules. Design and Fabrication: Fabrication Materials, Transistor Fundamentals, Fabrication Processes.

Module II (5 Hrs)

Partitioning: Levels of Partitioning, Partitioning Algorithms: Kernighan-Lin Algorithm, F-M Algorithm, Goldberg-Burstein Algorithm, Component Replication Algorithm, Ratio Cut Algorithm.

Module III (6 Hrs)

Floor planning: Floor Plans, Floor Planning problems, Sliceable Floor Plans: Slicing Trees, Normalized Postfix Notations, Rectangular Dualization, Non-Sliceable Floor Plans: Z-cuts, Sequence Pair, O-tree, Corner Block list, Twin Binary Sequence.

Module IV (6 Hrs)

Placement: Levels of Placement, Objectives, Placement for hi-performance systems, Methods for VLSI Placement: Cluster Growth, Partitioning based VLSI Placement Algorithm, Simulated Annealing, Simulated Evolution, Force-Directed method.

Module V (7 Hrs)

Routing: Objectives, Constraints, Design specifications, Steps of Routing, Phases of Routing. Global routing: Grid Graph Model, Checker's Board Model, Channel Intersection Graph Model, Global routing algorithms: Maze Routing Algorithms, Lee's Algorithm, Souk up's Algorithm, Line Probe Algorithm. Detailed routing: Routing region, Routing models, Terminologies, HCG, VCG, Two Layer Channels Routing Algorithms: Left Edge Algorithm, Constraint Graph based Routing Algorithms.

Course Outcomes:

CO1: Acquire knowledge about VLSI design, VLSI packaging style and fabrication.
CO2: Understand and select different partitioning algorithms for compact design.
CO3: Analyze and apply various floor planning techniques for efficient system design.
CO4: Evaluate for selection of efficient method for VLSI placement for performance aware design.
CO5: Able to design compact and performance aware VLSI devices with proper routing technique for efficient communication.

Essential Reading

1. Naveed A. Sherwani, "Algorithms for VLSI Physical Design Automation", Springer.

Supplementary Reading

1. D. Das, "VLSI Design", Oxford University press
2. M. Sarrafzadeh and C. K. Wong, "An Introduction to VLSI Physical Design" McGraw-Hill.
3. S. H. Gerez, "Algorithms for VLSI design automation", Wiley.