PET7J010 CMOS BASED DESIGN 3-0-0

MODULE-I (8 Hours)

Introduction to MOS Device-MOS Transistor, MOS models;MOS Transistor under static conditions; threshold voltage; Resistive operation, saturation region,;channel length modulation; body effect; DC transfer characteristics; Tristate inverters, velocity saturation; Hot carrier effect, drain current Vs voltage charts, sub threshold conduction; MOS structure capacitance; CMOS logic, fabrication and layout, stick diagrams.

MODULE-II (8 Hours)

CMOS Processing-CMOS technologies, wafer formation photolithography channel formation, isolation, gate oxide, gate source, drain formation, contacts and metallization; layout design rules, design rule checking.

MODULE-III (8 Hours)

Circuit Characterization & Performance Estimation-Delay estimation; transistor sizing; power dissipation; Sheet resistance, area capacitance, design margin, reliability; Scaling models, scaling factor for device parameters, Advantages and Limitations of scaling.

MODULE-IV (6 Hours)

Design of Combinational Logic-Static CMOS design, complementary CMOS, static properties, complementary CMOS design, Power consumption in CMOS logic gates, dynamic or glitching transitions, Design to reduce switching activity; Radioed logic, DC VSL, pass transistor logic.

ADDITIONAL MODULE (Terminal Examination-Internal) (6 Hours)

Differential pass transistor logic;sizing of level restorer, sizing in pass transistor; Dynamic CMOS design; Domino logic, optimization of Domino logic; NPCMOS; Designing logic for reduced supply voltages.

Reference Books

1. CMOS VLSI DESIGN-Nail H.E. Weste & David Harris, Ayan Banerjee,Pearson Education,4th edition,2011
2. CMOS Digital integrated circuits , Sung-Mo-Kanga and Yusuf Leblebici,TataMc Graw Hill New Delhi -2003.
3. Modern VLSI Design,Wayne Wolf, Prentice Hall -2nd Edition, 1998.
4. CMOS VLSI Design: A Circuits and Systems Perspective, Nail H.E. Weste & David Money Harris,- Addison Wesley, 3rd edition,2005.